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TITLE:

**IMPROVED MATERIALS FOR  
ELECTRONIC DEVICES**

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## IMPROVED MATERIALS FOR ELECTRONIC DEVICES

### 5 FIELD OF THE INVENTION

[0001] Improved materials for use in the fabrication of electronic devices comprising fillers with a negative coefficient of thermal expansion and components made therewith are described.

### 10 BACKGROUND INFORMATION

[0002] The construction of electronic devices involves the combination of a variety of materials exhibiting various mechanical and electrical properties. A designer or manufacturer of such devices may choose materials based in part on the mechanical and electrical properties of the materials in order to achieve performance and / or reliability in the devices.

[0003] Some materials used in electronic devices can be modified by adding fillers thereto. Fillers can be chosen to modify the rheological, thermal, and / or mechanical properties of the materials to which they are added. However, the use of fillers to advantageously modify one property can also introduce undesired modifications to one or more other properties in those materials. Thus, a manufacturer of electronic devices may be forced to choose a proportion of filler which is more or less than ideal with regard to one property in order to mitigate an adverse impact on other properties.

**[0004]** Electronic devices are frequently assembled from a semiconductor die and a next level package. The next level package may be, for example, a substrate, an interposer, a printed circuit board, or a printed wiring board.

Substrates may comprise a core upon which is built one or more layers of wiring

5 and build up dielectric. Substrates are typically formed with alternating layers of conductive material and build up dielectric material. Wiring patterns, commonly known as traces, may be built in the conductive material through various etching processes such as wet etching which are known in the art and will not be

described further herein. A semiconductor die may be joined with the next level

10 package by soldered interconnects and have an underfill agent disposed between them.

**[0005]** Electronic devices so constructed suffer from a number of stresses resulting from differing coefficients of thermal expansion in the various materials employed. For example, the substrate core may have a different coefficient of

15 thermal expansion than the build up dielectric layers. Similarly, the underfill agent may have a different coefficient of thermal expansion than the next level

package, the soldered interconnects, or the semiconductor die. The resulting stresses can lead to defects such as via delamination and corner fillet cracking in the underfill material, mechanical failures to the interconnects, and cracks in the

20 interlayer dielectric of the semiconductor die.

**[0006]** As previously mentioned, the coefficients of thermal expansion for some of the materials used in the construction of electronic devices can be modified by the addition of fillers. For example, the material used for the

substrate build up dielectric layer may be modified with a silica filler to reduce the coefficient of thermal expansion of the layer. Similarly, the underfill agent used in joining the semiconductor die with the next level package may be modified with a silica filler to reduce its coefficient of thermal expansion. However, known fillers  
5 may be inadequate to sufficiently modify these materials because heavily modified materials may exhibit poor flow characteristics and other undesirable properties. Thus, designers of electronic devices may be faced with using materials which have coefficients of thermal expansion greater than desired in order to retain in those materials other important qualities such as viscosity or  
10 filler loading. Hence, there is a significant need in the art for improved materials.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0007]** Figure 1 depicts part of a package for an electronic device according to an embodiment of the present invention, wherein substrate dielectric  
15 build up layers comprise a filler having a negative coefficient of thermal expansion.

**[0008]** Figure 2 depicts part of a package for an electronic device according to another embodiment of the present invention, wherein substrate dielectric build up layers comprise a filler having a negative coefficient of thermal  
20 expansion and wherein the filler loading has been reduced to yield different rheological properties.

**[0009]** Figure 3 depicts part of a package for an electronic device according to yet another embodiment of the present invention, wherein substrate

dielectric build up layers comprise a filler having a negative coefficient of thermal expansion and wherein the core material exhibits a low coefficient of thermal expansion.

5 [0010] Figure 4 depicts an embodiment of the present invention wherein a semiconductor die and a next level package have been bonded to form interconnects.

[0011] Figure 5 depicts an embodiment of the present invention wherein a semiconductor die and a next level package have been bonded and underfilled with an underfill material containing a filler having a negative coefficient of  
10 thermal expansion.

[0012] Figure 6 depicts another embodiment of the present invention wherein a semiconductor die and a next level package have been bonded and underfilled with an underfill material containing a filler having a negative coefficient of thermal expansion and wherein the filler loading has been reduced  
15 to yield different rheological properties.

[0013] Figure 7 depicts yet another embodiment of the present invention wherein a semiconductor die and a next level package have been underfilled with a no-flow underfill.

[0014] Figure 8 depicts a next level package according to the embodiment  
20 described in Figure 7.

[0015] Figure 9 depicts the next level package of figure 8 prepared for bonding to a semiconductor die.

**[0016]** Figure 10 depicts an electronic system containing one or more electronic devices according to an embodiment of the present invention.

#### DETAILED DESCRIPTION

5 **[0017]** In the following description numerous specific details are set forth. However, it is understood that embodiments may be practiced without these specific details. It is also understood that the description of particular embodiments is not to be construed as limiting the disclosure to those embodiments. Well-known circuits, structures and techniques have not been  
10 shown in detail in order not to obscure the understanding of this description.

**[0018]** As used herein, "filler" means any material used to modify another material by combination therewith. Fillers may be solids, liquids, slurries, powders, crystals or any other phase. Fillers may be a single substance or a combination of substances. Fillers may be present in any ratio, including forming  
15 the bulk of the modified material.

**[0019]** As used herein, "CTE" means coefficient of thermal expansion. A coefficient of thermal expansion may be described in a number of ways. One description uses the unit of measure "ppm/degree C", meaning parts-per-million per degree Centigrade. For example, a material having a CTE of 100ppm/degree  
20 C, when heated through a temperature change of 100 degrees Centigrade, will expand by (10,000/1,000,000), equivalent to a 1% expansion. The use of "CTE" and "ppm/degree C" in this disclosure is simply for explanatory purposes and no limitation is implied by the use of these terms.

**[0020]** As used herein, "negative CTE" means a coefficient of thermal expansion less than zero and "positive CTE" means a coefficient of thermal expansion greater than zero.

**[0021]** Reliability in electronic devices can be improved by employing materials with comparable coefficients of thermal expansion. The coefficient of thermal expansion of a silicon die may be approximately 3ppm/degree C. The coefficient of thermal expansion of a substrate may be 17ppm/degree C for a substrate having an FR4 core, or lower, such as approximately 8ppm/degree C one having an Alloy 42 core. Solder, frequently used for making mechanical and electrical connections between the die and the substrate, may have a coefficient of thermal expansion of approximately 28ppm/degree C. Unmodified build up dielectric material may have a coefficient of thermal expansion of approximately 100ppm/degree C. Unmodified underfill material may have a coefficient of thermal expansion of approximately 100ppm/degree C. Silica, a common positive CTE material used as filler, has a CTE of approximately 4 to 5ppm/degree C.

**[0022]** Figure 1 depicts a simplified view of part of a substrate 100 for an electronic device according to one embodiment of the present invention. Substrate 100 comprises core 110 and multiple layers of build up dielectric material 120 modified with a filler, the filler exhibiting a negative coefficient of thermal expansion.

**[0023]** Core 110 may be an organic material such as FR-4. FR-4 is a core having a woven glass mat and an epoxy resin. The coefficient of linear expansion for FR-4 is approximately 17ppm/degree C. Substrate 100 is also shown with

multiple layers of conductive material 130 having conductive traces. Conductive material 130 is preferably copper, though those skilled in the art will appreciate that the present invention is not limited by the choice of conductive material.

While Figure 1 depicts layers of build up dielectric 120 and layers of conductive

5 material 130 on two faces of core 110, those skilled in the art will understand that layers of materials 120 and 130 may instead be employed on only one face of core 110. Additionally, those skilled in the art will appreciate that more or fewer layers of materials 120 and 130 may be employed, and that additional layers or materials not shown may also be employed.

10 **[0024]** According to this embodiment of the present invention, build up dielectric material 120 preferably comprises an epoxy-acrylate binder filled with zirconium tungstate. Those skilled in the art will realize that the present invention is not limited to epoxy-acrylate binders, nor is it limited to zirconium tungstate, and that various other binders and negative CTE fillers may be used. Zirconium  
15 tungstate ( $\text{ZrW}_2\text{O}_8$ ) is a member of the class of compounds having the chemical composition  $\text{Zr}_x\text{W}_y\text{O}_z$ . Zirconium tungstate is a crystalline material having a nearly isotropic negative coefficient of thermal expansion, averaging approximately -8.8ppm/degree C over the temperature range of -273 to 127 degrees C for the alpha phase and averaging approximately -4.9ppm/degree  
20 Centigrade over the temperature range 157 to 677 degrees Centigrade for the beta phase. That is, zirconium tungstate has the property that it contracts when heated.



**[0025]** By modifying the epoxy-acrylate binder through the addition of zirconium tungstate, the coefficient of thermal expansion of build up dielectric layers 120 can be reduced to more closely match that of substrate 100. The effective coefficient of thermal expansion for build up dielectric material 120

5 comprising epoxy-acrylate and zirconium tungstate filler can be described by the rule of mixtures, wherein build up dielectric material 120 exhibits a coefficient of thermal expansion reflecting the relative amounts of the epoxy-acrylate and zirconium tungstate and their respective coefficients of thermal expansion.

**[0026]** The rule of mixtures is a formula used to predict the coefficient of

10 thermal expansion of a composite, based on known coefficients of thermal expansion of the individual components. A common form of the rule of mixtures for predicting the CTE of a two-component composite is the linear expression:

$\alpha_c = \alpha_1 + (\alpha_2 - \alpha_1) V_2$ , where  $\alpha_c$  is the composite CTE,  $\alpha_1$  and  $\alpha_2$  are the CTEs for component 1 and component 2, respectively, and  $V_2$  is the volume fraction of

15 the second component. From this description it is apparent that the coefficient of thermal expansion of build up dielectric material 120 can be reduced by raising the proportion of zirconium tungstate relative to epoxy-acrylate binder.

**[0027]** The use of a negative CTE filler at a given volume fraction loading will result in the modified build up dielectric material having a lower coefficient of  
20 thermal expansion than it would have if modified with a positive CTE filler at that same volume fraction loading. Thus, the use of a negative CTE filler will allow designers of electronic devices to modify the build up dielectric material to have a

lower coefficient of thermal expansion than could be achieved under like conditions using a filler having a positive CTE.

**[0028]** Figure 2 depicts a simplified view of a substrate 140 according to another embodiment of the present invention. Substrate 140 comprises core 150  
5 and multiple layers of build up dielectric material 120 modified with a filler, the filler exhibiting a negative coefficient of thermal expansion.

**[0029]** According to this embodiment of the present invention, core 150 comprises a metal having a low coefficient of thermal expansion, such as Alloy 42. Alloy 42 is a nickel-iron alloy having a coefficient of linear expansion of  
10 approximately 8ppm/degree C.

**[0030]** Substrate 140 is also shown with multiple layers of conductive material 130 having conductive traces. Conductive material 130 is preferably copper, though those skilled in the art will appreciate that the present invention is not limited by the choice of conductive material. While Figure 2 depicts layers of  
15 build up dielectric 120 and layers of conductive material 130 on two faces of core 150, those skilled in the art will understand that layers of materials 120 and 130 may instead be employed on only one face of core 140. Additionally, those skilled in the art will appreciate that more or fewer layers of materials 120 and 130 may be employed, and that additional layers or materials not shown may  
20 also be employed.

**[0031]** According to this embodiment of the present invention, build up dielectric material 120 preferably comprises an epoxy-acrylate binder filled with zirconium tungstate. Those skilled in the art will realize that the present invention

is not limited to epoxy-acrylate binders, nor is it limited to zirconium tungstate, and that various other binders and negative CTE fillers may be used.

**[0032]** In this embodiment, build up dielectric layers 120 have a coefficient of linear expansion which is more disparate to core 150 than they would have to an organic FR-4 core, since core 150 has a lower coefficient of thermal expansion than an organic FR-4 core. However, since the layers of build up dielectric material 120 are modified with zirconium tungstate, the CTE of build up dielectric material 120 will be closer to that of core 150 than would be the case when using a known build up material, such as one filled with silica. Thus, reliability in electronic devices comprising Alloy 42 or other low-CTE metal cores may be improved over the state of the art by using build up dielectric layers 120.

**[0033]** Figure 3 depicts a simplified view of substrate 160 for an electronic device according to yet another embodiment of the present invention. Substrate 160 comprises core 110 and multiple layers of build up dielectric material 170 modified with a filler, the filler having a negative coefficient of thermal expansion.

**[0034]** Substrate 160 is also shown with multiple layers of conductive material 180 having conductive traces. Conductive material 180 is preferably copper, though those skilled in the art will appreciate that the present invention is not limited by the choice of conductive material. Material 180 comprises conductive traces formed with a smaller line width than traces formed in the conductive material 130 described above. While Figure 3 depicts layers of build up dielectric 170 and layers of conductive material 180 on two faces of core 110, those skilled in the art will understand that layers of materials 170 and 180 may

instead be employed on only one face of core 110. Additionally, those skilled in the art will appreciate that more or fewer layers of materials 170 and 180 may be employed, and that additional layers or materials not shown may also be employed.

5    **[0035]**       According to this embodiment of the present invention, build up dielectric material 170 is preferably an epoxy-acrylate binder filled with zirconium tungstate. Here, build up dielectric material 170 is modified to a lesser degree than the previously-described build up dielectric material 120. That is, build up dielectric material 170 has a lower volume fraction filler loading than does  
10   material 120. Since modification with a negative CTE filler lowers the effective coefficient of thermal expansion of the build up dielectric material, modification to a lesser degree results in build up dielectric material 170 exhibiting a greater coefficient of thermal expansion than that of build up dielectric material 120. However, build up dielectric material 170 will nonetheless exhibit a lower  
15   coefficient of thermal expansion than would be the case when using a known dielectric material, such as one filled with an equal volume fraction loading of a positive CTE filler such as silica. Thus, by employing build up dielectric material 170 according to this embodiment of the present invention, the designer or manufacturer of an electronic device may obtain a build up dielectric material  
20   having the same coefficient of thermal expansion as currently known materials yet having a lower volume fraction filler loading.

**[0036]**       A number of benefits may follow from employing build up dielectric material 170. Since material 170 has a lower volume fraction filler loading, it may

exhibit improved rheological properties and enable improved substrate designs. Thus, substrate 160 may be designed with smaller features than would otherwise be used with previously known dielectric materials. For example, smaller features may be possible due to the reduced stresses in vias, resulting in the ability to go  
5 to smaller diameters and still have acceptable reliability.

**[0037]** It is well known in the art to apply dielectric build up layers in the form of photoactive spin-on dielectrics. Epoxy-acrylate spin-on dielectrics are applied in a liquid state and cured. Curing may occur through application of heat, light, catalysts, or other means. The photoactive nature of the spin-on dielectric  
10 material allows it to be exposed to light through a mask and developed using techniques well known in the art. The rheological properties of epoxy acrylate dielectrics are important to the design and manufacture of the electronic device, and these properties are affected by the volume fraction filler loading. Thus, for example, modifying a spin-on dielectric with a filler may increase the viscosity of  
15 the spin-on dielectric.

**[0038]** Employing build up dielectric material 170 will improve the ability to control the rheological properties of the dielectric material during processing, which may lead to improved reliability and manufacturability in substrate 160 and electronic devices constructed therefrom. As mentioned, the reduced volume  
20 fraction filler loading of material 170 may provide for a lower viscosity during application than would be obtained from a prior art material having the same CTE, such as material filled with silica, a positive CTE filler. This may then allow for improved adhesion between layers of materials 170 and 180 through

improved flow characteristics. For example, improved step coverage may be obtained by using the lower-viscosity material 170 than would be obtained with a prior art material having the same CTE, since the prior art material would contain more filler and thus be more viscous.

5    **[0039]**        Figures 4 and 5 depict another embodiment of the present invention wherein an underfill comprising a negative CTE filler is used to improve reliability in an electronic device. Figure 4 depicts an arrangement of a next level package and a semiconductor die. Arrangement 200 comprises a next level package, herein substrate 210. Although this embodiment describes using  
10    substrate 210 as a next level package, those skilled in the art will appreciate that the invention is not limited to substrates, and may be similarly employed with other types of next level packages including, but not limited to, interposers, printed wiring boards, or printed circuit boards. Arrangement 200 further comprises semiconductor die 220. Substrate 210 and semiconductor die 220 are  
15    joined by a plurality of interconnects 230.

**[0040]**        Figure 5 depicts the arrangement of Figure 4 after it has been modified by the addition of underfill material 240 into gap 215. Underfill material 240 contains a novel filler having a negative coefficient of thermal expansion, the filler preferably being zirconium tungstate.

20    **[0041]**        It is well known in the art that the reliability of electronic devices can be improved by the use of an underfill agent between the semiconductor die and the substrate. Underfill agents are frequently an epoxy material modified with a positive CTE filler such as silica. Underfill agents serve to improve the

mechanical strength of the bond between the semiconductor die and the substrate and which may also serve to protect the semiconductor die and / or substrate from exposure to environmental factors such as moisture. Typical epoxy materials are liquid until they are cured by application of heat, catalysts, or other means.

**[0042]** According to this embodiment of the present invention, underfill material 240 comprises a novel epoxy bonding agent filled with zirconium tungstate. Since zirconium tungstate has a negative coefficient of thermal expansion, averaging -1.2ppm/degree C, underfill material 240 exhibits a lower coefficient of thermal expansion than that of known underfill materials filled with an equal volume fraction loading of a positive CTE filler such as silica.

**[0043]** Electronic device 205 may exhibit improved reliability due to the presence of underfill material 240 because the coefficient of thermal expansion of underfill material 240 may more closely match that of the surrounding materials.

For example, the coefficient of thermal expansion of underfill material 240 may more closely match that of interconnects 230. Interconnects 230 may comprise solder having a coefficient of thermal expansion of approximately 28ppm/degree C. Underfill material 240 will exhibit a lower CTE than would a known underfill material filled with the same volume fraction loading of a positive CTE filler such as silica.

**[0044]** One technique for producing an underfill between a substrate and a semiconductor die is to apply the underfill material in a liquid state to a gap between the semiconductor die and the substrate. The liquid underfill then flows

between the semiconductor die and the substrate through natural forces such as capillary action. The liquid underfill may cure as it flows between the die and the substrate or may be cured subsequently. In either case, the rheological properties of the underfill material are important to obtaining the desired mechanical strength and isolation from environmental factors.

**[0045]** Figure 6 depicts part of an electronic device 260 according a different embodiment of the present invention, wherein arrangement 200 described in Figure 4 has been modified by the addition of underfill material 250. Underfill material 250 contains a filler having a negative coefficient of thermal expansion.

**[0046]** According to this embodiment of the present invention, underfill material 250 comprises an epoxy bonding agent filled with a filler having a negative coefficient of thermal expansion, preferably zirconium tungstate, wherein the volume fraction filler loading is less than that of the previously described underfill material 240. Since the volume fraction filler loading of underfill material 250 is somewhat less than that of underfill material 240, the coefficient of thermal expansion of material 250 will be somewhat greater than that of material 240. However, underfill material 250 may still exhibit a coefficient of thermal expansion which is equal to that of a known underfill material filled with a greater volume fraction loading of a positive CTE filler such as silica.

**[0047]** Since underfill material 250 may exhibit a coefficient of thermal expansion equal to that of known underfill materials while having a lower volume fraction loading, underfill material 250 may exhibit advantageous rheological



properties. One such property is reduced viscosity, which may be very important in underfilling. As mentioned above, one technique for producing an underfill involves applying the underfill material in a liquid state to a gap between the semiconductor die and the substrate. The viscosity of the underfill material is an  
5 important factor in the effectiveness of this technique, because an underfill material which is too viscous may leave excessive voids, which is detrimental to the mechanical and sealing functions the underfill is intended to provide. In Figure 6, underfill 250 is effective to achieve the mechanical and sealing functions.

10 **[0048]** Figures 7, 8, and 9 depict parts of an electronic device comprising a no-flow underfill according to another embodiment of the present invention. Figure 7 depicts part of an electronic device 300 comprising a semiconductor die 320, a next level package and an underfill. In this embodiment, next level package is substrate 330. Although this embodiment describes using substrate  
15 330 as a next level package, those skilled in the art will appreciate that the invention is not limited to substrates, and may be similarly employed with other types of next level packages including, but not limited to, interposers, printed wiring boards, or printed circuit boards. In this embodiment, the underfill is a no-flow underfill 310 containing a filler having a negative coefficient of thermal  
20 expansion, preferably zirconium tungstate. In this embodiment, no-flow underfill material 310 is applied to substrate 330 before substrate 330 is bonded to semiconductor die 320.

**[0049]** Figures 8 and 9 depict further details of electronic device 300 shown in Figure 7. Figure 8 depicts a more detailed view of substrate 330, showing connection points 340. Connection points 340 may comprise copper, a lead-tin eutectic, solder, or any other conductive material and are typically formed in an array or other regular pattern. Connection points 340 may be any shape including cylindrical, hemispherical, or mushroom shaped. Connection points 340 are formed on substrate 330 prior to application of no-flow underfill material 310 and prior to bonding with semiconductor die 320.

**[0050]** Figure 9 depicts a more detailed view of semiconductor die 320 and substrate 330 after application of no-flow underfill material 310 and prior to bonding substrate 330 with semiconductor die 320. Semiconductor die 320 has connection points 350 which may be in the form of pads or bumps and may comprise any conductive material. Connection points 350 are typically formed in an array or other regular pattern which matches that of connection points 340 on substrate 330.

**[0051]** Employing a no-flow underfill in an electronic device may allow the manufacturer to combine the interconnect bonding step with the underfill step, thereby reducing the number of steps required to build an electronic device and improving efficiency. For example, the reflow of the connection points and the cure of the underfill material may be combined into a single step. However, combining these steps can lead to other difficulties. One problem that may arise is poor connections between the substrate and the die as the result of material becoming trapped between the substrate connection points and the

semiconductor die connection points. This trapped material can impede the mechanical and electrical bonding of the connection points and result in electrical opens or other defects, thereby reducing manufacturing yield and increasing costs.

5     **[0052]**         According to this embodiment of the present invention, no-flow underfill material 310 is applied to substrate 330 before substrate 330 and semiconductor die 320 are bonded. Semiconductor die 320 and substrate 330 are brought into contact such that connection points 340 and connection points 350 are substantially aligned and touching.

10    **[0053]**         Die 320 and substrate 330 are then exposed to a heat source which causes connection points 340 and / or connection points 350 to melt, thereby bonding and forming interconnections between semiconductor die 320 and substrate 330. No-flow underfill material 310 may optionally include a fluxing agent to improve the bonding of connection points 340 with connection points  
15    350. Preferably, the heat source concurrently heats no-flow underfill material 310 causing it to cure. Once cured, no-flow underfill material 310 will improve the mechanical strength of the bond between semiconductor die 320 and substrate 330 and will help seal them against environmental factors.

**[0054]**         Since no-flow underfill material 310 is filled with zirconium tungstate  
20    filler, it can exhibit a coefficient of thermal expansion equivalent to that of a known no-flow underfill material, such as one filled with a positive CTE filler such as silica, but a lower volume fraction filler loading. Thus, material 310 may provide greater yields because reduced filler loading makes it less likely that

material 310 will become trapped between connection points 340 and connection points 350. A manufacturer employing underfill material 310 may experience fewer defects and greater yields than would be the case using previously known compounds filled with positive CTE materials.

5    **[0055]**       Figure 10 is a block diagram representing a simplified view of an electronic system comprising one or more electronic devices according to an embodiment of the present invention. Electronic system 400 includes an electronic component 410 which is electrically coupled to various components in electronic system 400 via system bus 420 and/or other cabling. Some  
10   interconnections between the various components are not shown in the interest of clarity. Electronic component 410 includes at least one semiconducting device, such as device 300 shown in FIG. 7. Electronic component 410 may optionally include a microprocessor, microcontroller, chip set, graphics processor or digital signal processor, and/or a custom circuit or an application-specific integrated  
15   circuit, such as a communications circuit. System bus 420 may be a single bus or any combination of busses.

**[0056]**       Electronic system 400 may also include an external memory 440 that in turn includes one or more memory elements suitable to the particular application, such as a main memory in the form of random access memory, one  
20   or more hard disc drives, and/or one or more drives that handle removable media such as floppy diskettes, compact discs or digital video discs.

**[0057]**       Electronic system 400 may also include a display component 450, an audio component 460, and one or more controllers 460, such as a keyboard,

mouse, joystick, scanner, or any other component that inputs information into the electronic system 400.

**[0058]** The foregoing detailed description and accompanying drawings are only illustrative and not restrictive. They have been provided primarily for a clear  
5 and comprehensive understanding of the disclosed embodiments and no unnecessary limitations are to be understood therefrom. Numerous additions, deletions, and modifications to the embodiments described herein, as well as alternative arrangements, may be devised by those skilled in the art without departing from the spirit of the disclosed embodiments and the scope of the  
10 appended claims.